

IN THE CLAIMS

Please amend the claims as follows.

1-15. (Canceled)

16. (Currently Amended) An integrated circuit (IC) package comprising:

a substrate having a substantially planar upper surface entirely throughout an IC mounting region and a plurality of conductors within the ~~the~~ IC mounting region on the upper surface;

at least one capacitor within the IC mounting region, wherein the at least one capacitor comprises top and bottom surfaces, each having a plurality of terminals of first and second polarity types, wherein a selected terminal of first polarity type on the bottom surface is physically and electrically coupled to a first conductor of the plurality of conductors, ~~and~~ wherein a selected terminal of second polarity type on the bottom surface is physically and electrically coupled to a second conductor of the plurality of conductors, and wherein the at least one capacitor is mounted atop and at a diagonal to the first and second conductors to which it is electrically coupled; and

an IC comprising a plurality of IC terminals on a surface thereof, wherein the IC terminals are physically and electrically coupled to selected terminals of first and second polarity types on the top surface of the capacitor.

17. (Previously Presented) The IC package recited in claim 16, wherein the first conductor is to couple to a first potential, and the second conductor is to couple to a second potential.

18. (Canceled)

19. (Previously Presented) The IC package recited in claim 16, wherein the at least one capacitor is mounted atop at least three conductors.

20. (Previously Presented) The IC package recited in claim 16, wherein the at least one capacitor is a capacitor array.

21. (Previously Presented) The IC package recited in claim 16, wherein the plurality of capacitor terminals are disposed over substantially the entire top and bottom surfaces.

22-25. (Canceled)

26. (Original) The IC package recited in claim 16, wherein the plurality of conductors are substantially parallel to one another.

27. (Canceled)

28. (Original) The IC package recited in claim 16 and comprising a plurality of capacitors distributed substantially throughout the IC mounting region, each capacitor being in electrical contact with at least one of the conductors.

29. (Canceled)

30. (Original) The IC package recited in claim 16, wherein the conductors include pads.

31-64. (Canceled)

65. (Previously Presented) An integrated circuit (IC) package comprising:

a substrate having a plurality of conductors within an IC mounting region, wherein the conductors include at least a first conductive bar having a height and a width, the height exceeding the width;

at least one capacitor within the IC mounting region and electrically coupled to the first conductive bar, wherein the at least one capacitor is mounted atop the first conductive bar; and

an IC electrically coupled to the plurality of conductors via the at least one capacitor.

66. (Previously Presented) The IC package recited in claim 65, wherein the at least one capacitor is further electrically coupled to a second conductive bar of the plurality of conductors, wherein the first conductive bar is to couple to a first potential, and wherein the second conductive bar is to couple to a second potential.

67. (Previously Presented) The IC package recited in claim 65, wherein the at least one capacitor has a top and a bottom, and wherein the at least one capacitor has terminals on its top and bottom.

68. (Previously Presented) The IC package recited in claim 65 and comprising a plurality of capacitors distributed substantially throughout the IC mounting region, each capacitor being in electrical contact with at least one of the conductors.

69. (Previously Presented) The IC package recited in claim 68, wherein the plurality of capacitors comprises a plurality of sets of capacitors, each set comprising two or more capacitors having ends and being aligned substantially end-to-end.

70. (Previously Presented) An integrated circuit (IC) package comprising:
a substrate having a plurality of conductors within an IC mounting region, wherein the conductors include at least a first conductive bar having a height and a width, the height exceeding the width;
a plurality of capacitors distributed substantially throughout the IC mounting region and electrically coupled to the first conductive bar, wherein the plurality of capacitors comprises a plurality of capacitor arrays; and
an IC electrically coupled to the plurality of conductors via the plurality of capacitors.

71. (Previously Presented) The IC package recited in claim 70, wherein selected ones of the plurality of capacitors are further electrically coupled to a second conductive bar of the plurality of conductors, wherein the first conductive bar is to couple to a first potential, and wherein the second conductive bar is to couple to a second potential.

72. (Previously Presented) The IC package recited in claim 70, wherein each of the plurality of capacitors has a top and a bottom, and wherein selected ones of the plurality of capacitors have at least one terminal on their top and at least one terminal on their bottom.

73. (Previously Presented) The IC package recited in claim 70, wherein each of the capacitor arrays has a top and a bottom, and wherein selected ones of the capacitor arrays have a plurality of terminals of first and second polarities on their top and a plurality of terminals of first and second polarities on their bottom.

74. (Previously Presented) The IC package recited in claim 70, wherein selected ones of the plurality of capacitor arrays are interdigitated capacitors.

75. (Previously Presented) An integrated circuit (IC) package comprising:

a substrate having a plurality of conductors within an IC mounting region, wherein the plurality of conductors are substantially parallel to one another, and wherein the plurality of conductors include at least a first conductive bar having a height and a width, the height exceeding the width;

a plurality of capacitors within the IC mounting region and electrically coupled to the first conductive bar, wherein the plurality of capacitors comprises a plurality of capacitor arrays; and

an IC electrically coupled to the plurality of conductors via the plurality of capacitors.

76. (Previously Presented) The IC package recited in claim 75, wherein selected ones of the plurality of capacitors are further electrically coupled to a second conductive bar of the plurality of conductors, wherein the first conductive bar is to couple to a first potential, and wherein the second conductive bar is to couple to a second potential.

77. (Previously Presented) The IC package recited in claim 75, wherein each of the plurality of capacitors has a top and a bottom, and wherein selected ones of the plurality of capacitors have at least one terminal on their top and at least one terminal on their bottom.

78. (Previously Presented) The IC package recited in claim 75, wherein each of the capacitor arrays has a top and a bottom, and wherein selected ones of the capacitor arrays have a plurality of terminals of first and second polarities on their top and a plurality of terminals of first and second polarities on their bottom.

79. (Previously Presented) The IC package recited in claim 75, wherein the plurality of capacitor arrays are non-orthogonally mounted atop the plurality of conductors.

80. (Previously Presented) The IC package recited in claim 79, wherein the conductors are diagonal to the plurality of capacitor arrays.

81. (Previously Presented) An integrated circuit (IC) package comprising:
a substrate having a plurality of conductors within an IC mounting region, wherein the plurality of conductors include at least a first conductive bar having a height and a width, the height exceeding the width;
a capacitor array within the IC mounting region and electrically coupled to the first conductive bar; and
an IC electrically coupled to the plurality of conductors via the capacitor array.

82. (Previously Presented) The IC package recited in claim 81, wherein the capacitor array is further electrically coupled to a second conductive bar of the plurality of conductors, wherein the first conductive bar is to couple to a first potential, and wherein the second conductive bar is to couple to a second potential.

83. (Previously Presented) The IC package recited in claim 81, wherein the capacitor array is non-orthogonally mounted atop the plurality of conductors.

84. (Previously Presented) The IC package recited in claim 81, wherein the capacitor array has a top and a bottom, and wherein the capacitor array has at least one terminal on its top and at least one terminal on its bottom.

85. (Previously Presented) The IC package recited in claim 84, wherein the capacitor array has a plurality of terminals of first and second polarities on its top and a plurality of terminals of first and second polarities on its bottom.

86. (Canceled)

87. (Previously Presented) The IC package recited in claim 82, wherein the at least first and second conductive bars have a gap to accommodate the capacitor array.

88. (Previously Presented) An integrated circuit (IC) package comprising:
a substrate having a plurality of conductors within an IC mounting region, wherein the conductors include at least one conductive bar having a height and a width, the height exceeding the width;
a plurality of capacitors within the IC mounting region, wherein the plurality of capacitors are mounted beside and in electrical contact with the at least one conductive bar; and
an IC electrically coupled to the plurality of conductors via the plurality of capacitors.

89. (Previously Presented) The IC package recited in claim 88, wherein the plurality of conductors comprises at least first and second conductive bars, wherein the first conductive bar is to couple to a first potential, and wherein the second conductive bar is to couple to a second potential.

90. (Previously Presented) The IC package recited in claim 88, wherein selected ones of the plurality of capacitors have a first side and a second side, wherein the first side comprises at least one terminal of first polarity, and wherein the second side comprises at least one terminal of second polarity.

91. (Previously Presented) The IC package recited in claim 88, wherein selected ones of the plurality of capacitors are mounted beside one of the plurality of conductors.

92. (Previously Presented) The IC package recited in claim 88, wherein selected ones of the plurality of capacitors are mounted between two of the plurality of conductors.

93. (Previously Presented) The IC package recited in claim 88, wherein the at least one conductive bar has a length, and wherein at least one of the plurality of capacitors has a length substantially the same as the length of the at least one conductive bar.

94. (Previously Presented) The IC package recited in claim 88, wherein the plurality of conductors comprises at least first and second conductive bars having a height and a width, the height exceeding the width, wherein the first conductive bar is to couple to a first potential, wherein the second conductive bar is to couple to a second potential, wherein the first and second conductive bars have a length, wherein at least one of the plurality of capacitors has a length substantially the same as the length of the first and second conductive bars and is mounted beside and in electrical contact with the first and second conductive bars, wherein at least another of the plurality of capacitors is a capacitor array, and wherein the at least first and second conductive bars have a gap to accommodate the capacitor array.

95. (Previously Presented) The IC package recited in claim 94, wherein the capacitor array has a top and a bottom, wherein the capacitor array has at least one terminal on its top and at least one terminal on its bottom, and wherein the at least one terminal on its bottom is coupled to one of the first and second conductive bars.

96. (Previously Presented) The IC package recited in claim 94, wherein the capacitor array is transverse to the at least one capacitor.

97. (Previously Presented) An integrated circuit (IC) package comprising:
a substrate having a plurality of conductive bars within an IC mounting region, the conductive bars having a height and a width, the height exceeding the width;
a plurality of capacitors within the IC mounting region, wherein the plurality of capacitors are mounted beside and in electrical contact with selected ones of the conductive bars;
and
an IC electrically coupled to the plurality of conductive bars via the plurality of capacitors.

98. (Previously Presented) The IC package recited in claim 97, wherein selected ones of the plurality of capacitors have a first side and a second side, wherein the first side comprises at least one terminal of first polarity, and wherein the second side comprises at least one terminal of second polarity.

99. (Previously Presented) The IC package recited in claim 98, wherein the IC comprises a plurality of pads of first and second polarities, wherein the selected ones of the plurality of capacitors have a top and a bottom, wherein at least one terminal on the top is of a first polarity, wherein at least one terminal on the top is of a second polarity, wherein the at least one terminal of first polarity is coupled to at least one corresponding pad of first polarity, and wherein the at least one terminal of second polarity is coupled to at least one corresponding pad of second polarity.

100. (Previously Presented) An integrated circuit (IC) package comprising:
a substrate having a plurality of conductors within an IC mounting region, wherein the conductors include at least one conductive bar having a height and a width, the height exceeding the width;
at least one capacitor within the IC mounting region, wherein the at least one capacitor is mounted beside and in electrical contact with the at least one conductive bar; and
an IC electrically coupled to the plurality of conductors.
101. (Previously Presented) The IC package recited in claim 100, wherein the at least one capacitor is mounted between and electrically coupled to first and second conductive bars.
102. (Previously Presented) The IC package recited in claim 101, wherein the first conductive bar is to couple to a first potential, and wherein the second conductive bar is to couple to a second potential.
103. (Previously Presented) The IC package recited in claim 101, wherein the capacitor comprises terminals on two sides, and wherein the terminals are electrically coupled to the first and second conductive bars, respectively.
104. (Previously Presented) The IC package recited in claim 100, wherein the plurality of conductors are substantially parallel to one another.
105. (Previously Presented) An integrated circuit (IC) package comprising:
a substrate having a plurality of conductors within an IC mounting region, wherein the plurality of conductors are substantially parallel to one another;
a plurality of capacitors within the IC mounting region and electrically coupled to at least one of the conductors, wherein the plurality of capacitors comprises a plurality of capacitor arrays, and wherein the plurality of capacitor arrays are non-orthogonally mounted atop the plurality of conductors; and
an IC electrically coupled to the plurality of conductors via the plurality of capacitors.

106. (Previously Presented) The IC package recited in claim 105, wherein the plurality of conductors are substantially parallel to one another.

107. (Previously Presented) The IC package recited in claim 105, wherein the plurality of conductors are diagonal to the plurality of capacitor arrays.

Please add new claims 108-115 as follows:

108. (New) An integrated circuit (IC) package comprising:

a substrate having a substantially planar upper surface entirely throughout an IC mounting region and a plurality of conductors within the IC mounting region on the upper surface;

a plurality of capacitors distributed substantially throughout the IC mounting region, wherein each capacitor comprises top and bottom surfaces, each having a plurality of terminals of first and second polarity types, wherein a selected terminal of first polarity type on the bottom surface of each capacitor is physically and electrically coupled to a first conductor of the plurality of conductors, wherein a selected terminal of second polarity type on the bottom surface of each capacitor is physically and electrically coupled to a second conductor of the plurality of conductors; and

an IC comprising a plurality of IC terminals on a surface thereof, wherein the IC terminals are physically and electrically coupled to selected terminals of first and second polarity types on the top surface of the capacitor.

109. (New) The IC package recited in claim 108, wherein the plurality of capacitors comprises a plurality of sets of capacitors, each set comprising one or more capacitors aligned substantially end-to-end.

110. (New) The IC package recited in claim 108, wherein the first conductor is to couple to a first potential, and the second conductor is to couple to a second potential.

111. (New) The IC package recited in claim 108, wherein at least one capacitor is mounted atop at least three conductors.

112. (New) The IC package recited in claim 108, wherein at least one capacitor is a capacitor array.

113. (New) The IC package recited in claim 108, wherein the plurality of capacitor terminals are disposed over substantially the entire top and bottom surfaces.

114. (New) The IC package recited in claim 108, wherein the plurality of conductors are substantially parallel to one another.

115. ((New)) The IC package recited in claim 108, wherein the conductors include pads.